Understanding the transport of voltage-induced quantum dots in nanowire channel field-effect-transistors

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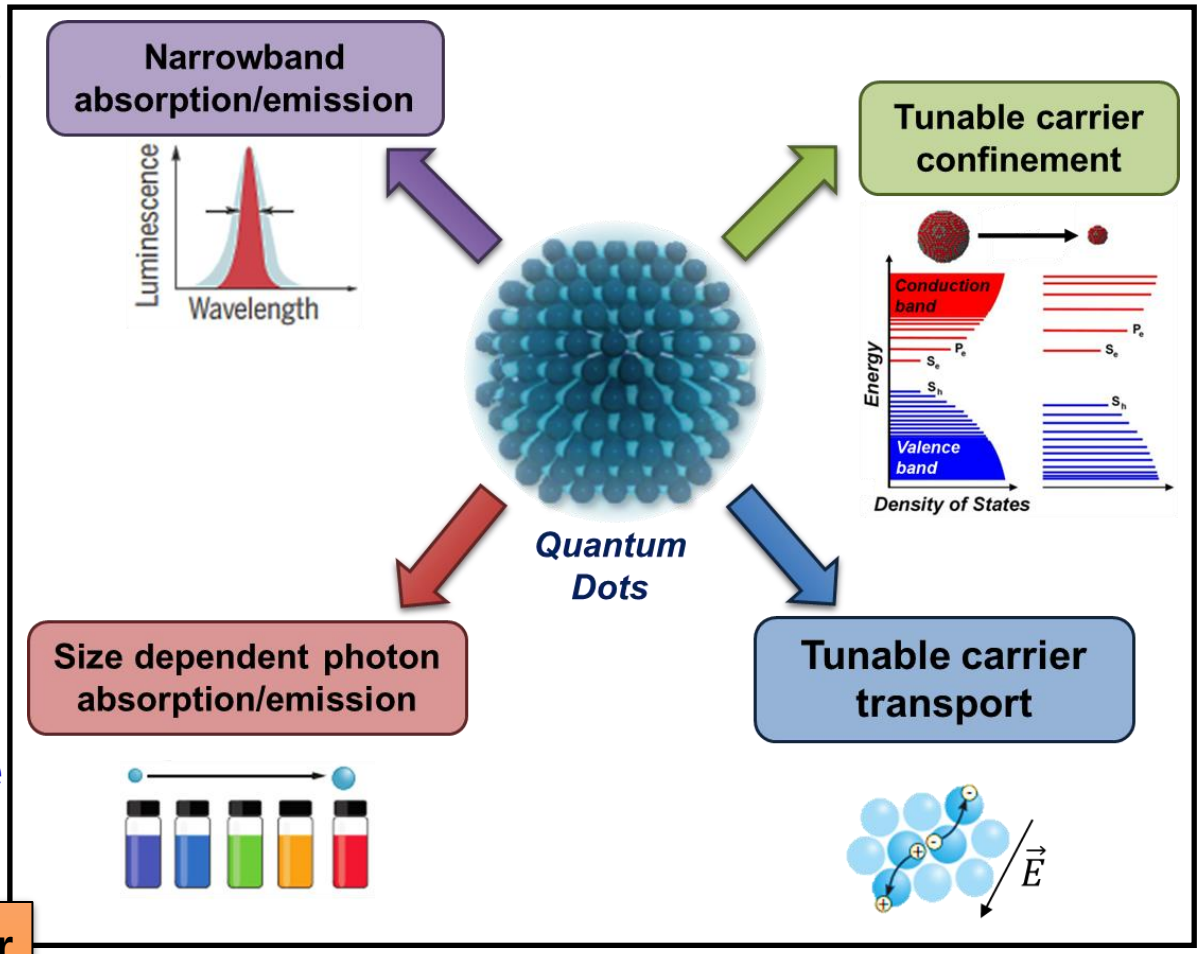
Outline

- Introduction: Quantum Dots (QDs).
- QDs for next-gen electronic devices.
- Progress and challenges of QDs.
- QD generation in nanowire FET.
- Mathematical modeling.
- Results.
- Conclusions.
- Acknowledgements.
- References.

Introduction: Quantum Dots

- QDs are material systems which confine charge carriers in 3-dimensions.
- Physical dimensions smaller than the de Broglie wavelength of charge carriers.
- Exhibit size dependent confinement.
- Atom-like energy states.
- Therefore, exhibit tunable transport properties.



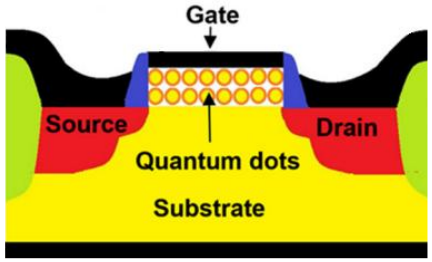
Tremendous potential for next-generation low-power electronic and quantum devices.

Kagan et. al., *Science 353,* aac5523 (2016).
DOI: *10.1126/science.aac5523*

García de Arquer et. al., *Science 373*, eaaz8541 (2021).
DOI: 10.1126/science.aaz8541

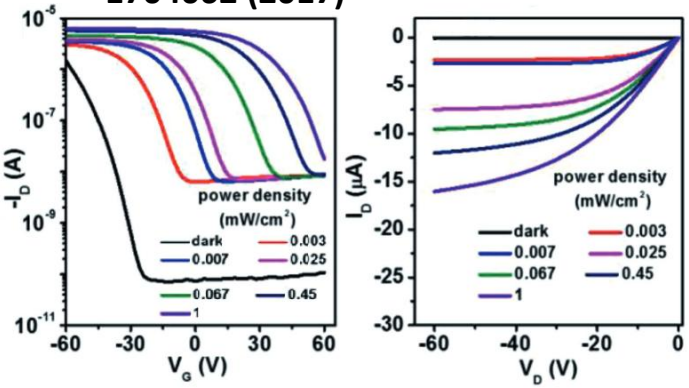
QDs for next-gen electronic devices

Solution processed QDs



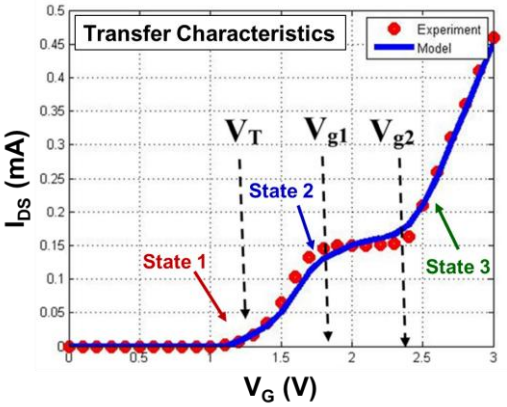
Solution processed QDs dispersed in the gate stack of planar transistors.

Chen et. al., *Adv. Mater. 29*, pp. 1704062 (2017)



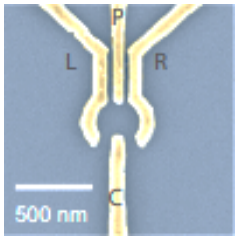
Wavelength sensitive photo-transistors.

Karmakar et. al., *Silicon 14*, pp. 12553-12565 (2022)



Multi-threshold devices for multiple logic levels.

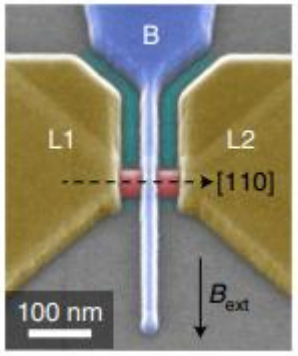
Gate-defined quantum dots



Kulesh et. al., *Phys. Rev. App. 13*, 041003 (2020)

Gate voltages create QDs by depleting 2D electron gas.

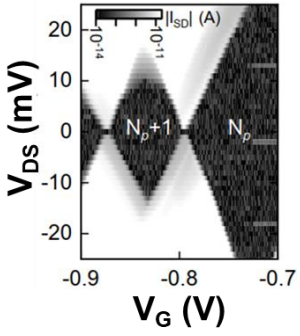
Quantum dots in FET architecture



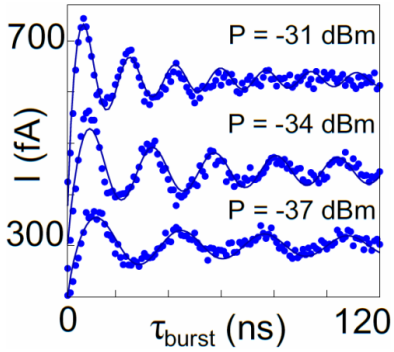
Camenzind et. al., *Nat. Electron. 5*, pp. 178-183 (2021)

Gate voltage along channel creates QDs within the channel.

Kuhlmann et. al., *Appl. Phys. Lett. 113 (12)*, pp. 122107 (2018)



Nadj-Perge et. al., *Nature 468*, pp. 1084–1087 (2010)



Integer charge confinement, charge oscillations for qubit generation.

QDs: Progress & Challenges

Challenges of solution processed QDs:

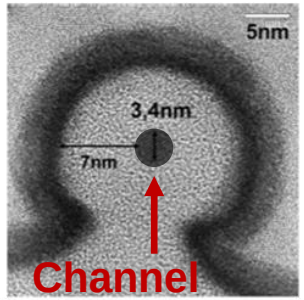
- **Transport properties significantly depend on QD size.**
- **Can introduce device to device variability, not ideal at large-scale.**
- **Not CMOS compatible.**

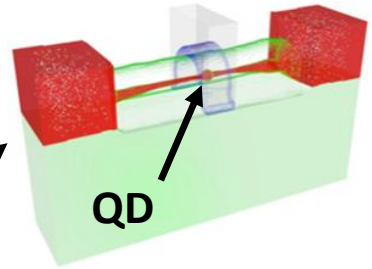
Challenges of gate defined QD devices.

- **QD sizes are limited by lithography processes, which lead to ~meV energy level spacing.**
- **Extremely susceptible to environmental noise.**
- **Operation limited to ~mK temperatures.**

Motivation for QDs in FET devices:

- **Channel dimensions are already at quantum length scale.**
- **Localized gates and spacers can create QDs.**
- **The dimensions can be further tuned for high temperature operation.**
- **CMOS compatible technology.**



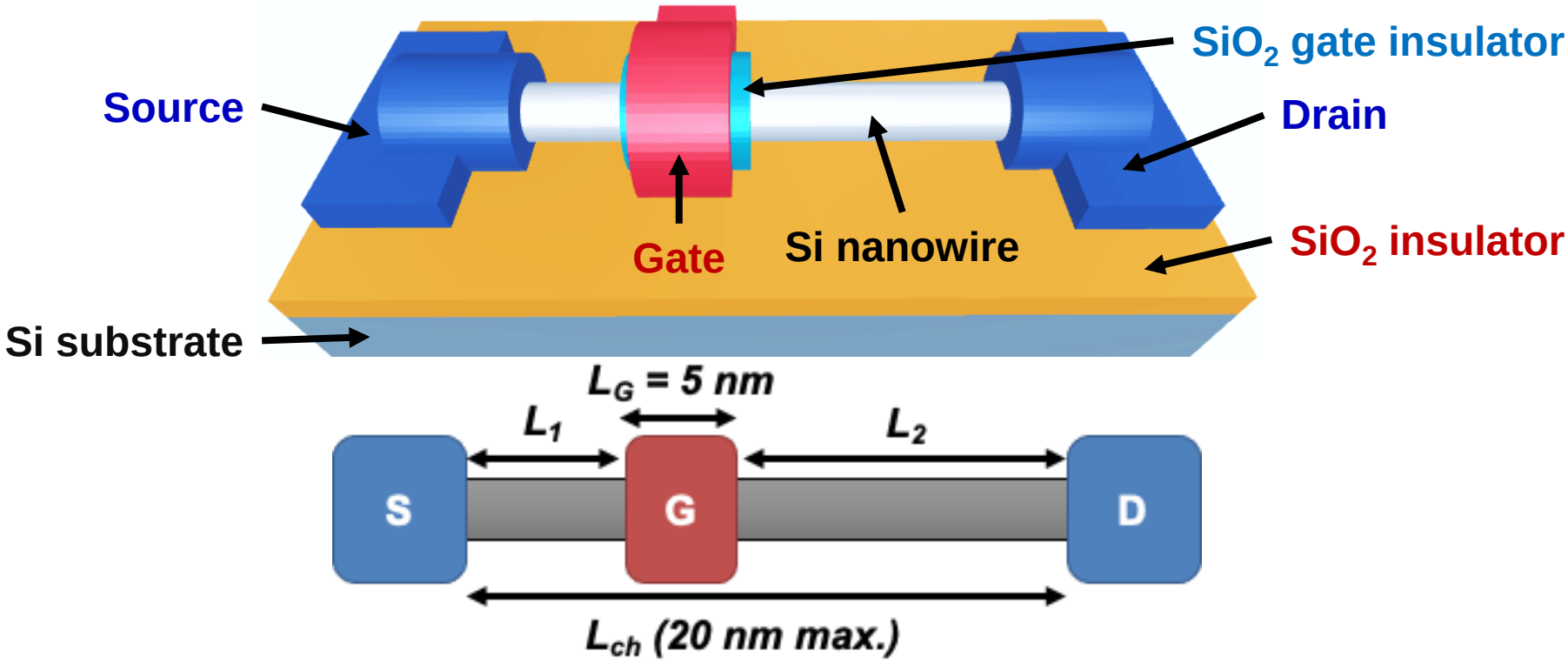


But current state-of-the-art uses several gates/spacers or constrictions (random) along the channel to realize the QDs!

Lavieville et. al., *Nanoletters 15(5)*, 2015

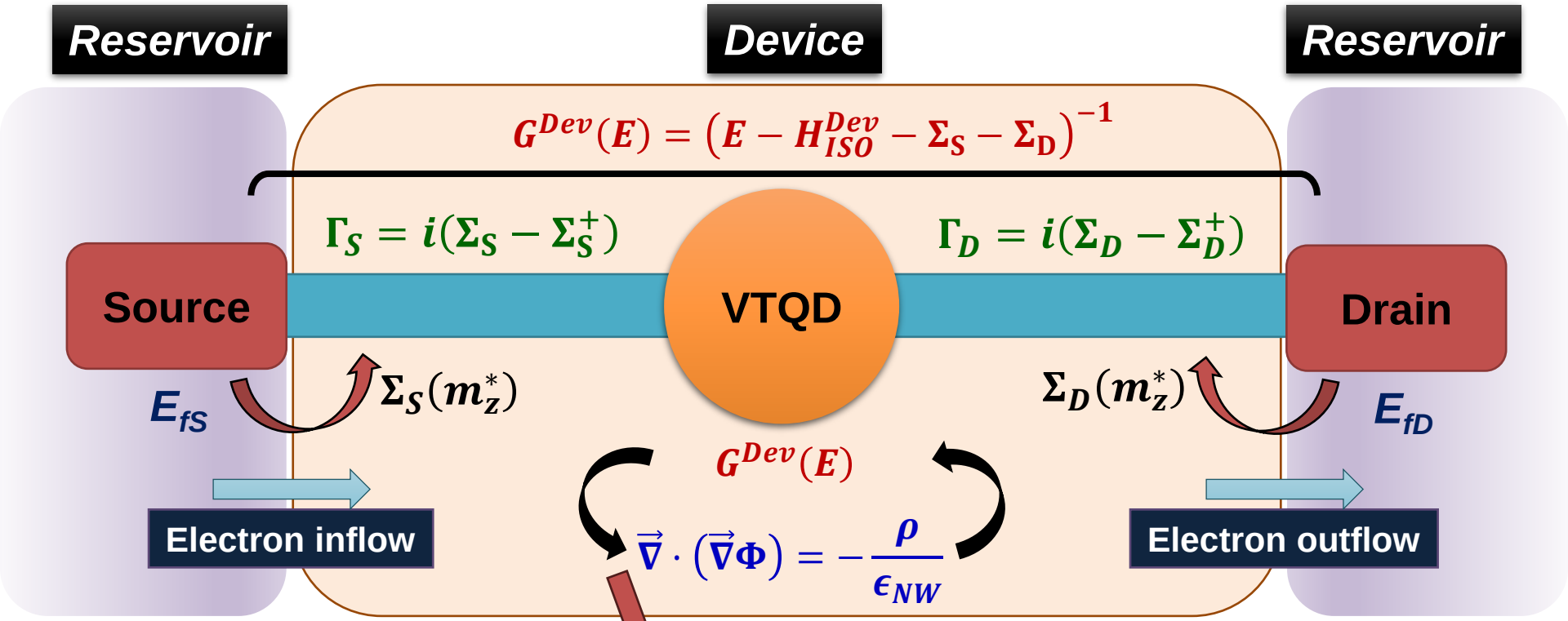
QD generation in NWFET

- Use localized gates to create voltage-tunable QDs (VTQDs) in the channel of a nanowire FET.
- Gate voltage controls electron population inside the VTQD.
- Gate voltage also modulates tunneling through the VTQD.
- Gate length and nanowire diameter control the overall VTQD eigenstates.



Schematic of the considered QD in state-of-the-art nanowire FET.

Mathematical Modeling: NEGF



$$\text{EOMs} \begin{cases} i\hbar \frac{dC_i}{dt} = H_{ISO}^{Dev} C_i + \tau_{ir} C_r \\ i\hbar \frac{dC_r^S}{dt} = H_S C_r^S + \tau_{ri}^{S*} C_i \\ i\hbar \frac{dC_r^D}{dt} = H_D C_r^D + \tau_{ri}^{D*} C_i \end{cases}$$

$$T(E) = \Gamma_S(E) G(E) \Gamma_D(E) G^+(E) \Rightarrow I = \frac{2e}{h} \int T(E)(f_S - f_D) dE$$

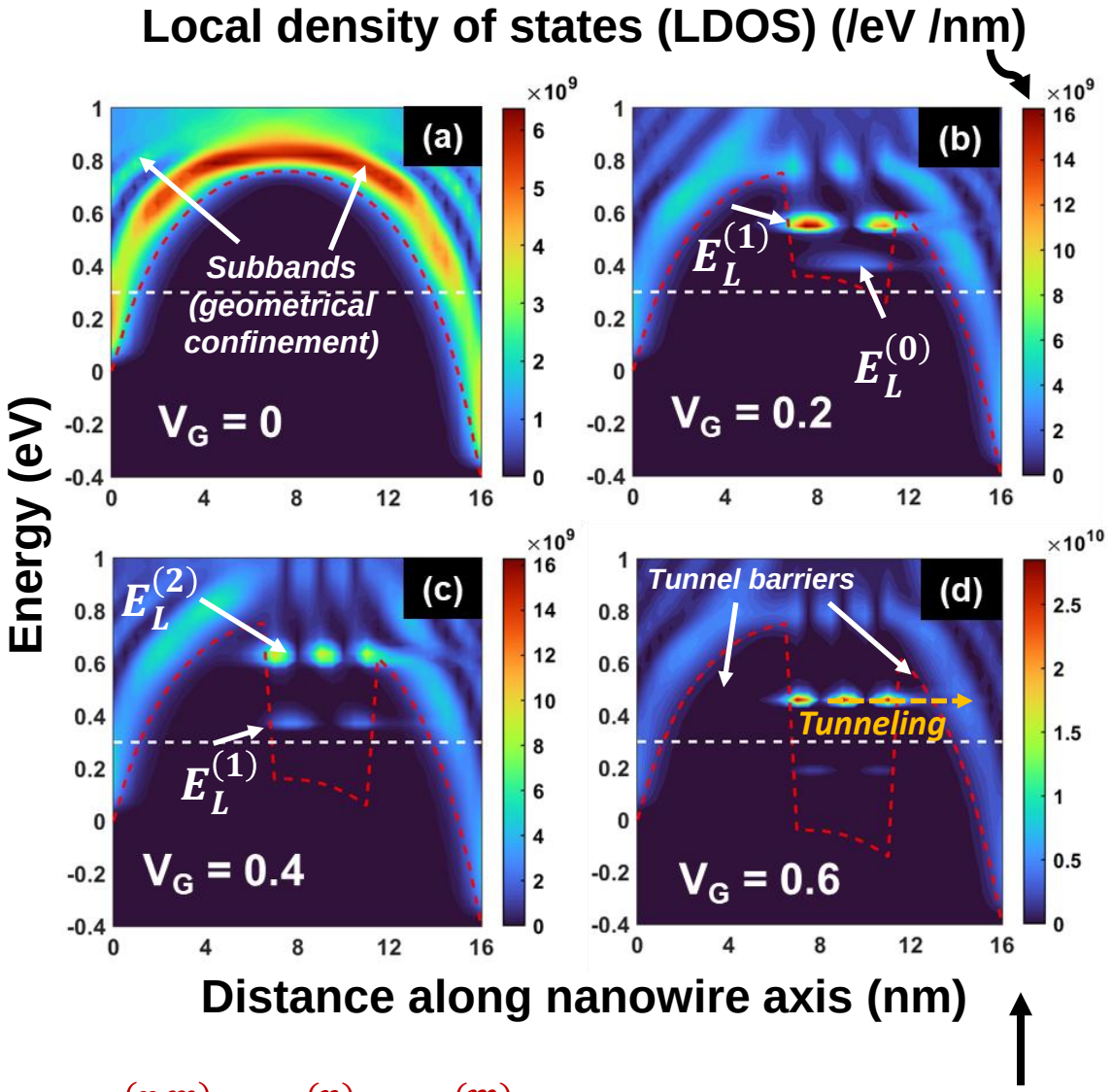
Note:

H_{ISO}^{Dev} is formulated using mode space approach.

$$H_{ISO} = -\hbar^2 \frac{\partial}{\partial z}\left(\frac{1}{m_z^*}\frac{\partial}{\partial z}\right) + E_{Sub} + U(z)$$

Results: LDOS

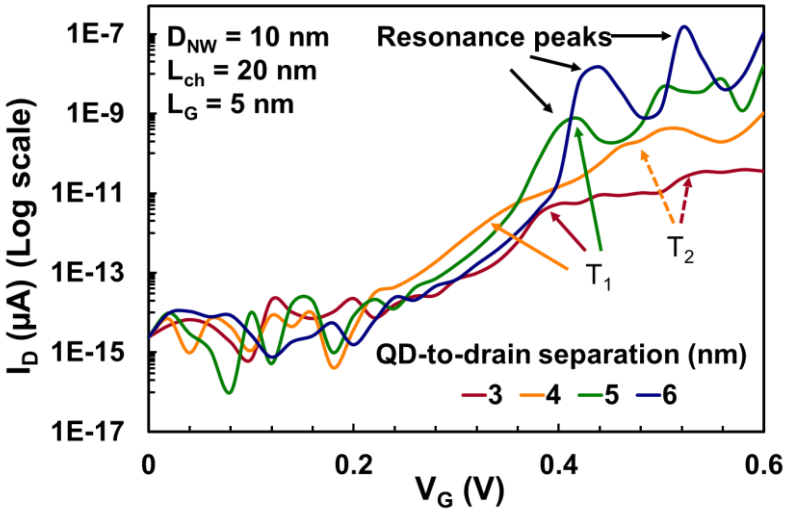
- Applying gate voltage creates localized potential well and the source/drain tunnel barriers.
- 5 nm gate length ensures electron confinement in the well.
- Higher V_G increases well depth to create stronger confinement.
- Higher V_G also manifests the higher energy eigenstates.
- Occupation of an eigenstate depends on the source fermi level, E_{fS}.
- Voltage induced confinement + geometrical confinement (nanowire geometry) = VTQD. $\longrightarrow E_{QD}^{(n,m)} = E_{sub}^{(n)} + E_L^{(m)}$

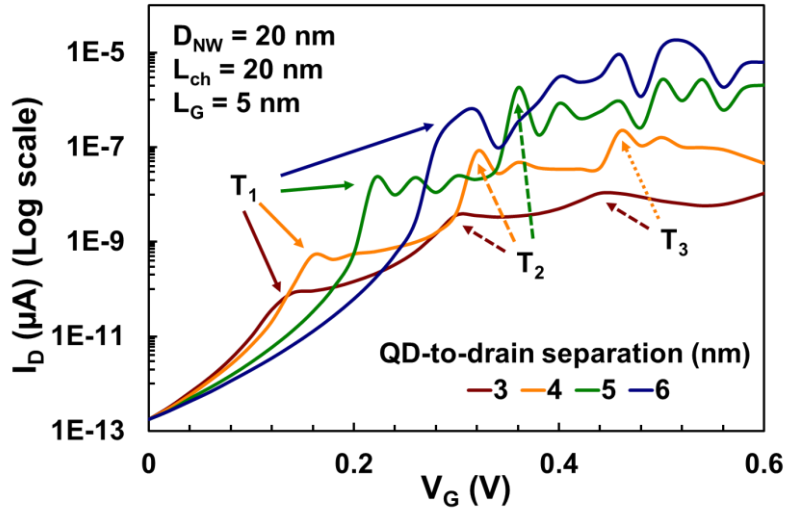


Note: $V_D = 0.4$ V

Results: Impact of QD-to-drain separation (L_2)

- Two extreme cases: strong (D_{NW} = 10 nm) and weak (D_{NW} = 20 nm) geometrical confinements explored.
- Transfer characteristics exhibit peaks corresponding to resonant tunneling.
- Decreasing the QD-to-drain separation increases broadening of the peaks, to lead to current thresholds, T_1, T_2… due to drain induced level-broadening.
- Increase in nanowire diameter from 10 nm to 20 nm leads to lowered tunnel barriers and weaker geometrical confinement of electrons.
- Thus, thresholds appear at a lower gate voltage (0.18 V) in such devices.
- Larger level broadening in such devices apparent as significantly broadened peaks in the transfer characteristics.

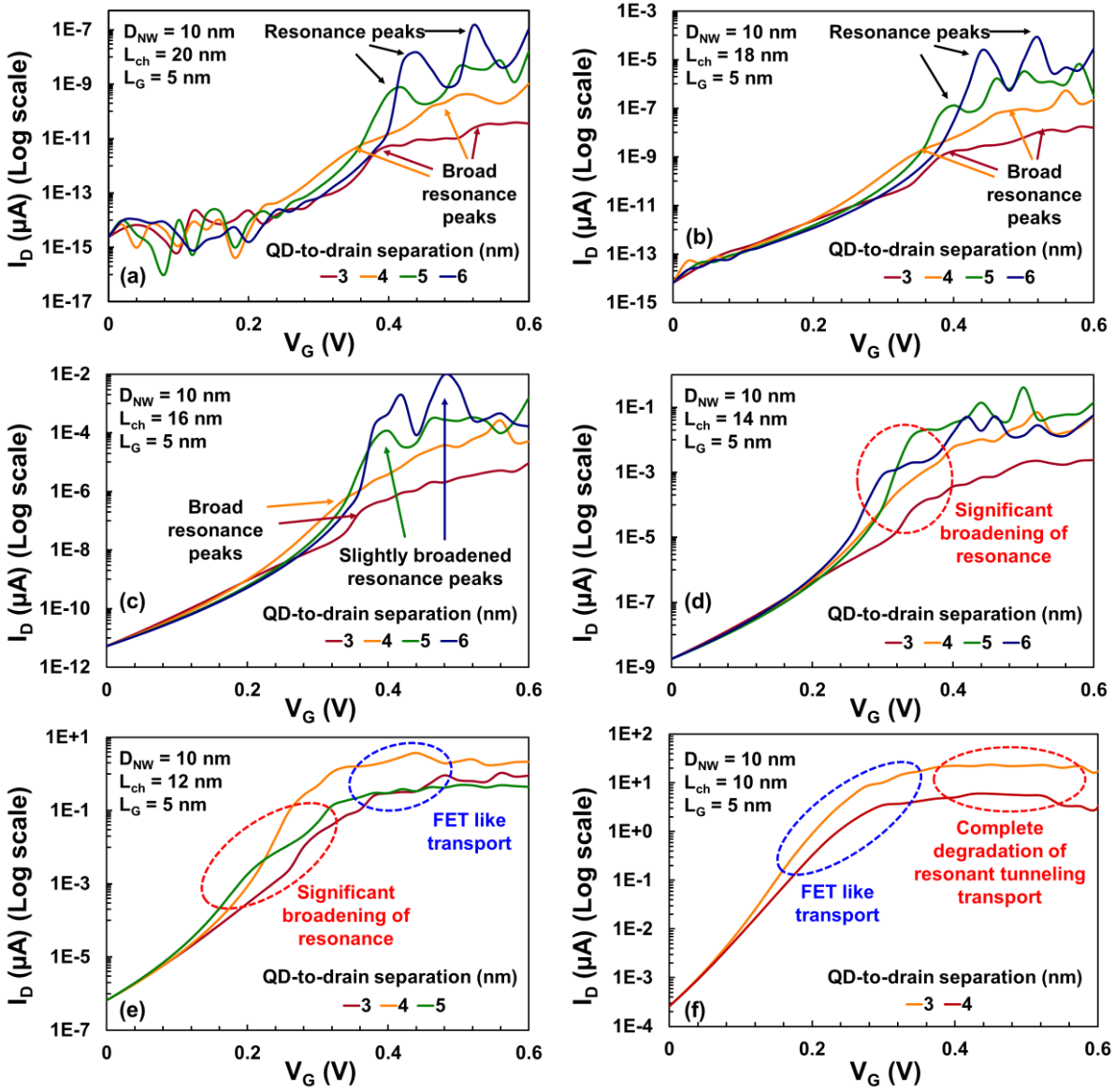




L_{ch} = 20 nm

Results: Impact of channel length (L_{ch})

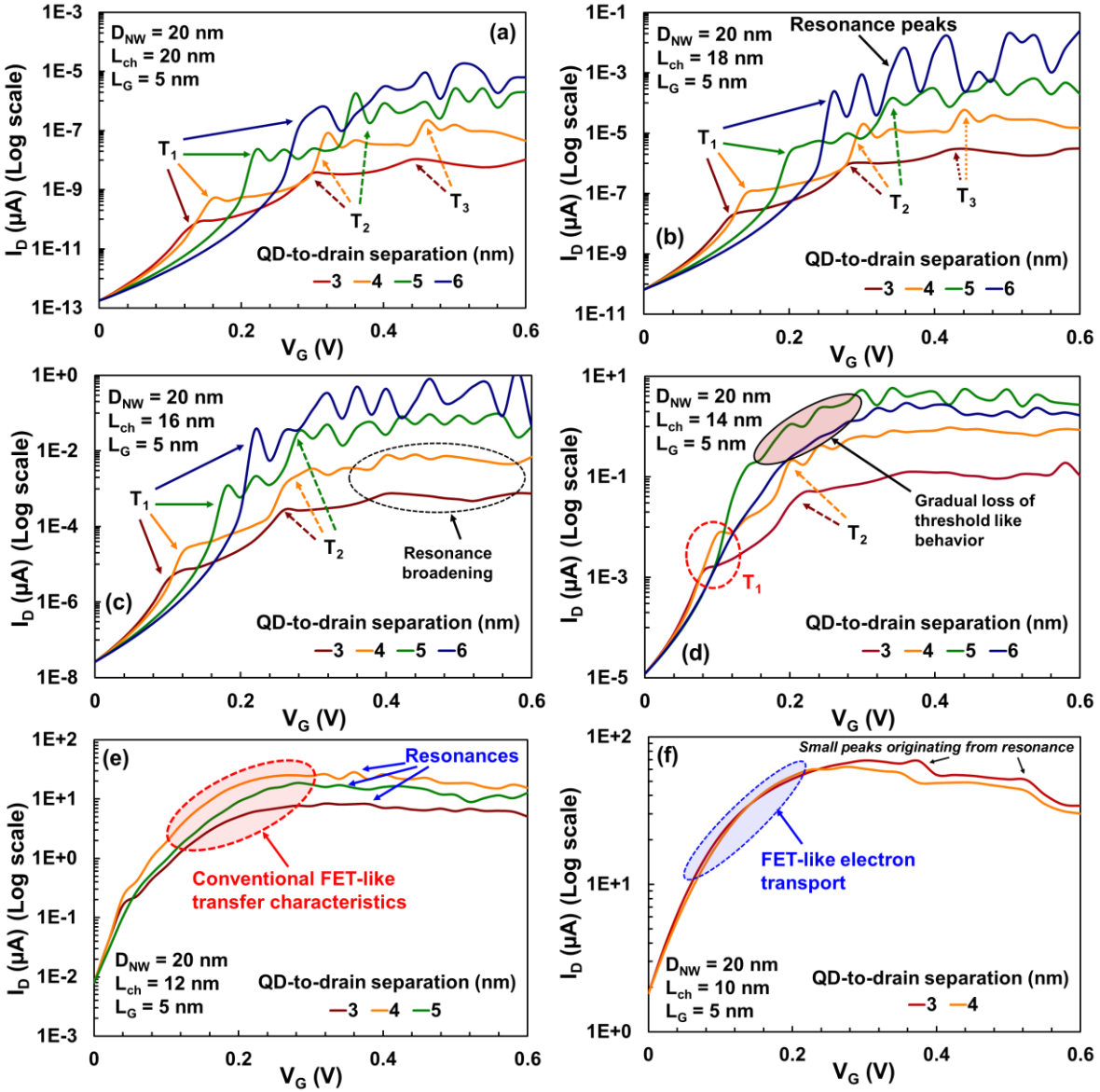
- Current levels increase with decreasing L_{ch}.
- For QD-to-drain separation $\leq$ 4 nm, the peaks undergo significant broadening due to increased coupling with the drain.
- The decrease in channel length also broadens the resonances.
- For L_{ch} < 14 nm, resonant tunneling features in transfer characteristics are substantially degraded.
- Conventional FET like transfer characteristics apparent for device with L_{ch} = 10 nm irrespective of QD position.



L_{ch}: 10 – 20 nm, QD-to-drain separation: 3 – 6 nm, D_{NW}: 10 nm.

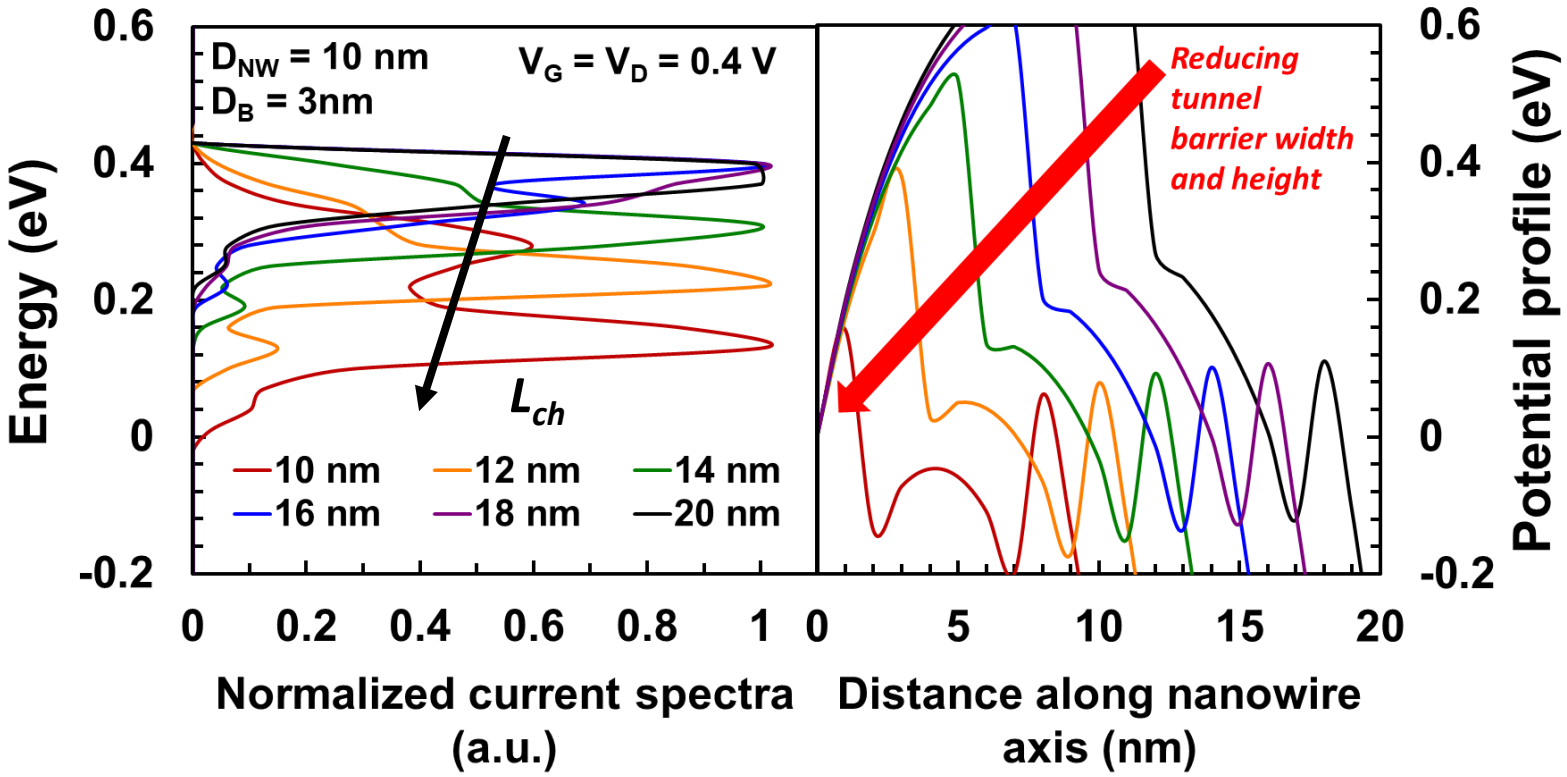
Results: Impact of channel length (L_{ch})

- Increased broadening of current peaks due to lowered potential barriers.
- For QD-to-drain separation < 6 nm, this broadening leads to several thresholds.
- Threshold like nature gradually disappears with the decrease in L_{ch}.
- For $L_{ch} \leq 12$ nm, the thresholds completely disappear to lead to conventional FET like transport.
- Conventional FET like transfer characteristics appears irrespective of QD position.



L_{ch}: 10 – 20 nm, QD-to-drain separation: 3 – 6 nm, D_{NW}: 20 nm.

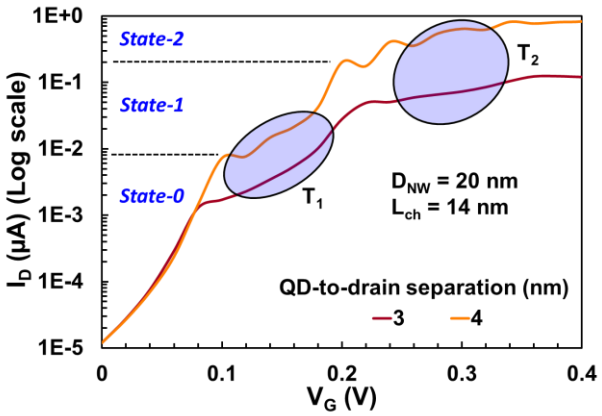
Results: Current spectrum



- Sharp peaks in current spectrum indicate energies at which conduction from source to drain occurs.
- Reducing the channel length lowers the peak energy since the barrier height and width also reduces.
- For L_{ch} ~ 10 nm, the secondary peak at ~0.3 eV (E_{fS}) leads to thermionic transport, which contributes to the FET-like transfer characteristics.

Conclusions

- Localized gates in nanowire FET devices with existing 2D geometrical confinement can create VTQDs along with voltage-induced tunnel barriers.
- The VTQD eigenstates are significantly affected by the position of gate along the channel, as well as the channel length.
- At larger QD-to-drain separations, sharp peaks in the transfer characteristics indicate the presence of sharp QD levels.
- Energy level broadening at smaller QD-to-drain separations lead to current thresholds. Devices in such configuration can be used as multi-threshold devices at room temperature.
- However, the VTQD behavior strongly depends on channel length. L_{ch} < 14 nm significantly degrades the QD characteristics as transport becomes thermionic.



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