Nilayan Paul, M.Sc.
UGC-Senior Research Fellow,
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Educational Qualifications:

- UGC-Senior Research Fellow (Dec., 2024 – Till date): Department of Electronic Science, University of Calcutta, Kolkata, India.
- UGC-Junior Research Fellow (Nov., 2022 – Nov., 2024): Department of Electronic Science, University of Calcutta, Kolkata, India.
- Project Assistant (Nov., 2021- Oct., 2022): Department of Electronic Science, University of Calcutta, Kolkata, India.
- M. Sc. Physics (2019-2021); Rajabazar Science College, University of Calcutta, Kolkata, India. (*Specialization: Solid State Electronics, Quantum Electronics, Microwave)*
- B. Sc. Physics (2016-2019); St. Xavier's College (Autonomous), Kolkata, India.

Present Status:

1. Presently working on modeling the transport phenomena of single and multi-quantum dot systems in gated nanowire FETs, using Non-Equilibrium Green's Function (NEGF) formalism, for quantum computing and next generation electronics devices.
2. Growth of composite oxide thin films by low-temperature VLS technique and their electrical/physical characterization.

Skills:

- Experienced in Python and MATLAB for scientific computing.
- Experience with working in class-100 clean room.
- Have work experience in operating Scanning Electron Microscope (Zeiss Auriga), EBSD (Oxford Instruments) and electron-beam lithography (Raith Elphy Plus).
- Experienced in operating thermal deposition system for thin film deposition.

- Experience in semiconductor device characterization (C-V, I-V and four probe resistivity measurements, including low temperature characterization (Ecopia)).
- Material characterization using Spectroscopic Ellipsometry (Sentech SE850) and absorption spectroscopy (Perkin Elmer λ-1050).

Book Chapters:

1. **Nilayan Paul**, Basudev Nag Chowdhury, Sanatan Chattopadhyay. *Investigating the Impact of Ge-Quantum Well Width in Si/SiO_2/Ge/SiO_2/Pt Resonant Tunneling Device with NEGF Formalism.* **In: Giri, C., Iizuka, T., Rahaman, H., Bhattacharya, B.B. (eds) Emerging Electronic Devices, Circuits and Systems.** Lecture Notes in Electrical Engineering, vol 1004. Springer (2023).

Publications in Peer Reviewed International Journals:

1. **Nilayan Paul**, S. Chattopadhyay. *Understanding the Nanowire Material-Dependent Charge Qubit Performance of Voltage-Tunable Double Quantum Dot Gate Nanowire Channel Field-Effect Transistors (DQD-NWFETs)*. Journal of Electronic Materials, p. 1 – 13 (2025). (IF 2.2)
   DOI: https://doi.org/10.1007/s11664-025-12059-3
2. **Nilayan Paul**, S. Chattopadhyay. *Design and modeling of resonant tunneling transport-controlled voltage-induced double quantum dot channel nanowire field-effect-transistor (DQD-FET) for multi-threshold current levels*. Solid-State Electronics (2025). (IF 1.4)
   DOI: https://doi.org/10.1016/j.sse.2025.109259
3.

Publications in Peer Reviewed International Conferences /Symposia /Workshops:

1. **Nilayan Paul**, Basudev Nag Chowdhury, Sanatan Chattopadhyay. *Investigating the impact of Ge-quantum well width in Si/SiO_2/Ge/SiO_2/Pt resonant tunneling device with NEGF formalism*, **5th International Symposium on Devices, Circuits and Systems (ISDCS)**, 2022.
2. **Nilayan Paul**, Basudev Nag Chowdhury, Sanatan Chattopadhyay. *Understanding the composition dependent charge qubit operations in a dual-gate $Al_xGa_{1-x}As$ nanowire FET using NEGF approach*, **XXII International Workshop on Physics of Semiconductor Devices (IWPSD),** 2023.
3. **Nilayan Paul**, Sanatan Chattopadhyay. *Understanding the material dependent charge qubit performance of voltage-tunable double quantum channel nanowire FETs.* **2nd International Conference on Low Energy Devices (ICLED)**, 2024.
4. **Nilayan Paul**, Sanatan Chattopadhyay. *Understanding the transport of voltage-induced quantum dots in nanowire channel field-effect-transistors.* **1st International Conference on Sustainable Technologies (ICST)**, 2024.

Pre-prints:

1. **Nilayan Paul**, Basudev Nag Chowdhury, Sanatan Chattopadhyay. *Design aspects of dual gate GaAs nanowire FET for room temperature charge qubit operation: A study on diameter and gate engineering*. (URL: https://doi.org/10.48550/arXiv.2304.10554)

2. **Nilayan Paul,** Sanatan Chattopadhyay. *Analytical Modeling of Resonant Tunneling Transport in a Voltage-Induced Double Quantum Dot Channel Nanowire FET for Multi-Threshold Current Levels.* (URL: https://ssrn.com/abstract=4926769)

Awards:

- UGC Junior Research Fellowship, 2022 - 2024.
- Best presentation award, ICLED-2024.
- UGC Junior Research Fellowship, 2024 onwards.

Other information:

- Developed custom Hall effect/resistivity measurement setup for room temperature measurements.